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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,379	FOSSUM, ERIC R.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: M4065.0628/P628-B
Filing Date: 4/20/2004
Claimed Priority Date: 8/29/2002 (Continuation of 10/230,079)
Applicant(s): Fossum
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 7/19/2005.

Acknowledgment

1. The amendment filed on 7/19/2005 has been entered. The directions, however, in page 4, line 12 of the amendment were defective. The instructions call for an amendment of paragraph [0043], when the correct place of entry should have been paragraph [0047]. Likewise, the status identifier of claim 46 should have been "Currently amended" instead of "Previously amended" as indicated in page 7 of the amendment. The examiner has corrected the amendatory paper according to MPEP § 714.23 to reflect the correct paragraph number and status identifier. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 35-48.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters **654** (see, *e.g.*, par.0047/ll.14) and **600** (see, *e.g.*, fig. 10) have both been used to designate the same processor.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in par.0039/ll.17 of the description in reference to a conductor: **131**.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 35, 36, 38, and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhao (US 6339248).

7. Regarding claim 35, Zhao (see, *e.g.*, fig. 8) shows all aspects of the instant invention including a pixel comprising:

- ✓ A substrate **101**
- ✓ A photoconversion device fabricated in the substrate **101**
- ✓ A charge collection region **103** of the device
- ✓ A reset region **123** of a first conductivity type in the substrate **101** and coupled to the collection region **103** for resetting the collection region in response to a signal applied to the reset region (see, *e.g.*, col.5/ll.30-34)

8. Regarding claim 36, Zhao shows the reset region **123** and the collection region **103** both forming an extended charge collection region (see, *e.g.*, fig. 8), the extended charge collection region also being reset by the applied signal (see, *e.g.*, col.5/ll.30-34).

9. Regarding claim 38, Zhao shows the pixel further comprising a pulsed voltage source periodically resetting the reset region and the charge collection region (see, *e.g.*, col.5/ll.30-34).

10. Regarding claim 40, Zhao shows the first conductivity type is n-type (see, *e.g.*, fig. 8).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Initially, and with respect to claims 37 and 42, note that a limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims and the functional limitations are found to be inherent in the prior art device. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best,

> Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

13. **Note that the applicant has burden of proof** once the examiner establishes a sound basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

14. Claims 37 and 42, 43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao in view of Chen (US 6392263).

15. Regarding claim 37, Zhao shows most aspects of the instant invention (see, *e.g.*, paragraphs 7 and 8 above) including:

✓ A source follower transistor **151** for outputting a signal representing charge collected in the extended collection region

✓ A row select transistor **153** for selectively outputting a signal from the source follower transistor **151**

Zhao also shows the source follower transistor **151** in electrical communication with the extended charge collection region, but fails to show a capacitor in electrical communication with the reset channel region **123** and the charge collection region for storing charge collected in the collection region. Chen, however, teaches that doing so would reduce the charge injection effect of Zhao's reset switch (see, *e.g.*, col.6/ll.59-61).

It would have been obvious at the time of the invention to one of ordinary skill in the art to include a capacitor in electrical communication with the reset region and the extended charge collection region, as suggested by Chen, to reduce the charge injection effect of Zhao's reset switch.

16. In reference to the language in claim 37 referring to the function of the capacitor, it is noted that Zhao/Chen show all aspects of the semiconductor device according to the claimed invention (see paragraph 25 above) and that using the capacitor to store charge collected in the collection region is a function that does not affect the structure of the final device. Furthermore, Zhao/Chen's device performs the claimed functions. That is, the carriers generated by the incoming light detected by the photodiode will be stored at the capacitor since one of its plates is directly connected to the photodiode node.

17. Regarding claim 42, Zhao (see, *e.g.*, fig. 8) shows most aspects of the instant invention including a pixel for use in an imaging device, the pixel consisting essentially of:

- ✓ A charge collection region **103**
- ✓ A reset region **123** adjacent the charge collection region **103** for periodically resetting a charge level of the collection region **103** in response to an applied reset signal (see, *e.g.*, col.5/ll.30-34)
- ✓ A source follower transistor **151** for outputting a signal representing charge collected in the collection region **103**
- ✓ A row select transistor **153** for selectively outputting a signal from the source follower transistor **151**

Zhao also shows the source follower transistor **151** in electrical communication with the reset region **123**, but fails to show a capacitor in electrical communication with the reset channel region **123** and the source follower transistor **151** for storing charge collected in the collection region. Chen, however, teaches that doing so would reduce the charge injection effect of Zhao's reset switch (see, *e.g.*, col.6/ll.59-61).

It would have been obvious at the time of the invention to one of ordinary skill in the art to include a capacitor in electrical communication with the reset region and the source follower transistor, as suggested by Chen, to reduce the charge injection effect of Zhao's reset switch.

18. In reference to the language in claim 42 referring to the function of the capacitor, it is noted that Zhao/Chen show all aspects of the semiconductor device according to

the claimed invention (see paragraph 27 above) and that using the capacitor to store charge collected in the collection region is a function that does not affect the structure of the final device. Furthermore, Zhao/Chen's device performs the claimed functions. That is, the carriers generated by incoming light detected by the photodiode will be accumulated at the capacitor since one of its plates is directly connected to the photodiode node.

19. Regarding claim 43, Zhao shows the reset region **123** and the collection region **103** both forming an extended charge collection region (see, *e.g.*, fig. 8). Zhao also shows (see, *e.g.*, col.5/ll.30-34) a voltage source resetting the extended collection region.

20. Regarding claim 45, Zhao shows the reset region **123** is doped with an n-type dopant at a first dopant concentration (see, *e.g.*, fig. 8).

21. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao in view of Kochi (US 6670990).

22. Regarding claim 39, Zhao shows most aspects of the instant invention (see, *e.g.*, paragraphs 7-9 above), except for the voltage source coupled to one terminal of a capacitor, the other terminal of which is coupled to the extended charge collection region. Kochi, on the other hand, teaches that doing so would enable Zhao's source follower to operate linearly, *i.e.*, to output a voltage in proportion to the input voltage (see, *e.g.*, col.16/ll.12-14 and col.2/ll.48-50). This would avoid signal deterioration associated with input/output linearity problems in low luminosity regions (see, *e.g.*, col.3/ll.7-8).

It would have been obvious at the time of the invention to one of ordinary skill in the art to include a capacitor having one terminal coupled to Zhao's voltage source and the other terminal coupled to the extended charge collection region, as suggested by Kochi, to avoid input/output linearity deterioration of the source follower in low luminosity regions.

23. Claims 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao/Chen in view Dasgupta (US 6146939).

24. Regarding claims 41 and 44, Zhao/Chen show most aspects of the instant invention (see, *e.g.*, paragraphs 25 and 28 above) including a capacitor in electrical communication with the reset region and the source follower transistor. As taught by Dasgupta, every capacitor has a capacitance per unit area associated with it. This capacitance may range from 4.3-5.3 $fF/\mu m^2$ depending on the choice and thickness of the capacitor dielectric (see, e.g., Dasgupta, col.1/ll.37 and col.3/ll.13-19). Zhao/Chen, however, fail to specify that the capacitance per unit area of the capacitor is between about 5-10 $fF/\mu m^2$. However, the specific capacitance values claimed will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such values are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicant has not established the criticality (see next paragraph) of the capacitance values claimed, and since these values are in common use in similar

devices in the art, as taught by Dasgupta, it would have been obvious to one of ordinary skill in the art to use these values in the device of Zhao/Chen.

CRITICALITY

25. The specification contains no disclosure of either the critical nature of the claimed mole ratio or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

26. Claims 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao/Chen in view of Wada (US 6677676).

27. Regarding claims 46-48, Chen shows the capacitor **450** is connected to the reset region **307** through an n-type contact region having a second dopant concentration (see, *e.g.*, fig. 4). Chen also shows the second dopant concentration **307** is higher than a first dopant concentration **405**. Chen, however, fails to show the contact region having a higher concentration than the reset region **123**. Wada, on the other hand, teaches that doing so would establish a good electrical connection between the capacitor and the reset region (see, *e.g.*, col.12/ll.28-31).

It would have been obvious at the time of the invention to have Zhao/Chen's contact region having a higher concentration than the reset region, as suggested by Wada, to establish a good electrical connection between the capacitor and the reset region.

Response to Arguments

28. The applicant argues:

N+ regions 123 and 125 of Zhao are "source and drain of the reset transistor" (col.4/ll.64-65), and not "a reset region...coupled to the charge collection region for resetting the charge collection region in response to

a signal applied to the reset region," as in the claimed invention. For at least these reasons, Zhao fails to anticipate the subject matter of claims 35, 36, 38, and 40.

The examiner responds:

The fact that diffusion region **123** is a source/drain region of Zhao's reset transistor does not oppose the fact that is also a reset region coupled to the charge collection region **103** for resetting the charge collection region **103** in response to a signal applied to the reset region **123**. See, *e.g.*, col.4/ll.16-26 and col.5/ll.29-34 of Zhao.

29. The applicant argues:

None of the reference shows "a capacitor in electrical communication with the reset channel region and the source follower transistor", as claim 42 recites.

The examiner responds:

In figure 4, Chen clearly shows a capacitor **450** in electrical communication with a reset channel region **307** and a source follower transistor **332**. See also figure 1C.

30. The applicant argues:

Kochi is silent about any of the limitations of claim 35. Kochi does not even mention, "a photoconversion device fabricated in said substrate".

The examiner responds:

See line 1 of the abstract and figures 7-12 and 17.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

35. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status

information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

36. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/59,72,222,223,225,228-234,290-294,431-466	8/15/05
Other Documentation: PLUS Analysis	8/15/05
Electronic Database(s): EAST (USPAT, EPO, JPO)	8/15/05

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MDP/mdp
August 15, 2005

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Art Unit 2814

[0043] The pixel is also reset before and after signal integration. Referring to Figures 7 and 8 during reset, the normally high voltage Vpd coupled to capacitor 171 from reset signal source 176 is pulsed low, e.g., to zero volts. This causes the charge within reset region 199 to effectively move upwardly in the direction of arrow A such that charges within channel 199 spill over barrier 147 into n+ region 142 which is connected to Vdd. Thus, charges are ejected from the photodiode region 126 and the reset region 199 and into n+ region 142 connected to Vdd. Vpd is then returned to a high value, for example 3.3 V, allowing charge integration to occur. This integrated charge is then read out in the manner described above. The barrier potential 147 is set to allow an anti-blooming operation to occur when charges collected on capacitor 171 in region 199 exceed the barrier potential [[145]] 147. This excess charge spills over to n+ region 142.

MDP
8/15/2005

[0047]

Please amend paragraph [~~0048~~] of the specification as follows:

[0047] A processor based system, such as a computer system, for example generally comprises, in addition to a CMOS imager 642 input device, a central processing unit (CPU) 644, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 646 over a bus 652. The CMOS image sensor 642 also communicates with the processor system over bus 652 or over other conventional communication path. The computer system 600 also includes random access memory (RAM) 648, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 654, and a compact disk (CD) ROM drive 656 or a flash memory card [[657]] which also communicate with CPU 644 over the bus 652. It may also be desirable to integrate the processor 654, CMOS image device 642 and memory 648 on a single IC chip.

43. (Currently amended) A pixel as in claim 42, wherein said reset region functions with said charge collection region as an extended charge collection region, and wherein a ~~said~~ voltage source ~~resetting~~ resets said extended charge collection region.

44. (Previously presented) The pixel of claim 42, wherein said capacitor has a charge-per-unit area capacitance value of about 5 to about 10 fF/μm2.

45. (Previously presented) The pixel of claim 42, wherein said reset region is doped with an n-type dopant at a first dopant concentration.

MDP 8/15/2005 (Currently amended)

46. ~~(Previously presented)~~ The pixel of claim [[42]] 45, wherein said capacitor is connected to said reset region through a contact region.

47. (Previously presented) The pixel of claim 46, wherein said contact region is doped with an n-type dopant at a second dopant concentration.

48. (Previously presented) The pixel of claim 47, wherein said second dopant concentration is higher than said first dopant concentration.